Gp 2816
4/Response
P. Wilke
10-22-02

PATENT
Attorney Docket No. 70803

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
David Glen Roe

Group Art Unit: 2816

Application No. 09/814,244

Examiner: COX, CASSANDRA F.

Filed: March 21, 2001

For: METHOD AND APPARATUS FOR PROVIDING MULTIPLE CLOCK SIGNALS ON A CHIP USING A SECOND PLL LIBRARY CIRCUIT CONNECTED TO A BUFFERED REFERENCE CLOCK OUTPUT OF A FIRST PLL LIBRARY CIRCUIT

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service on the date shown with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on October 2, 2002.

Kirk D. Williams, Esq.

REMARKS A

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In response to the non-final Office action mailed July 17, 2002, please consider the following remarks. Reconsideration and/or further prosecution of the application is respectfully requested.

The Office action dated July 17, 2002, and the reference cited therein have been carefully considered. Applicants traverse all rejections for at least the reasons stated herein after. Moreover, applicant requests allowance of all claims as the prior art of record neither teaches nor suggests the invention recited in the pending claims.

The following remarks reference the same numbered paragraphs of the Office action to which they are directed.

Paragraph 2. Claims 15 was rejected under 35 USC § 112, 2nd paragraph as being indefinite for the stated reason that the phrase "designing a circuit" is unclear, and claims 16-17 were rejected as they depend from independent claim 15.

Applicant traverses this rejection as the applicant sets forth in the specification that which applicant regards as his invention. "A fundamental principle contained in 35 USC § 112, second paragraph is that applicants are their own lexicographers." MPEP § 2173.01. Moreover, such a rejection "is only appropriate where applicant has stated, somewhere other than in the application as filed, that the invention is something different than what is defined by the claims. In other words, the invention set forth in the claims must be presumed, in the absence of evidence to the contrary, to be that which applicants regard as their invention." MPEP § 2172(I).

The specification, at least on page 9, line 12, recites that "FIG. 3 illustrates one embodiment of a process for *designing a circuit* for generating a first and a second clock reference signals," (*emphasis added*), and the language of FIG. 3A closely tracks that of claim 15. Applicants regard this as their invention, and make no assertions to the contrary. Moreover, the word "designing" includes many definitions such as, but not limited to "creating for a particular purpose." *See,* THE AMERICAN HERITAGE DICTIONARY OF THE ENGLISH LANGUAGE, (Third ed., Houghton Mifflin Company, 1992). For at least these reasons, applicant traverses the § 112, second paragraph rejections of claims 15-17, and requests these rejections be withdrawn.

As a further note, the preamble of claim 15 merely states an intended use of the invention as defined by claim 15, and does not limit the scope of the claim. In other words, "designing" is merely language of intended use, not a claim limitation. *See,* Loctite Corp. v. Ultraseal Ltd., 228 USPQ 90, 94 (Fed. Cir. 1985).

Paragraph 4. Claims 1-20 stand rejected under 35 USC 103(a) as being obvious over the "Phase-Locked Loop" IBM reference ("IBM reference") in view of Ho, US Patent 6,240,152.

Applicants traverse these rejections as the Office action fails to establish a primia facie case of obviousness as the IBM reference, alone or in combination with Ho, neither teaches nor suggests all the claim elements and limitations as required by the MPEP. The burden is on the Office Action to establish a prima facie case of obviousness, which has not been done as the MPEP requires, *inter alia*, that:

> "the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure."

MPEP § 706.02(j) (*citing In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991))(emphasis added).

Applicant agrees with the Office action that the "IBM reference does not disclose that the buffered reference clock output (BUFREFCLK) of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input (REFCLK) of the second phase-locked loop circuit (PLL7SLIBI)." Moreover, applicants submit that the IBM reference teaches away from such a combination as recited in independent claim 1. The IBM Reference, at least on page 843, teaches that the REFCLK of PLL7SLIBI "typically connects to the output of a receiver. Any receiver in the library may be used (differential or single-ended) provided that it is located in a test I/O slot." In other words, the IBM reference teaches that the REFCLK of PLL7SLIBI is connected to an I/O receiver (e.g., for receiving an off-chip signal), and not to another component, such as BUFREFCLK of a first phase-locked loop circuit.

The Office action cites Ho, lines 23-27, as teaching to overcome this Office action admitted deficiency of the IBM reference. Ho, lines 23-27 states:

> Phase-locked loop circuits are widely used in electronic systems. These circuits are used to generate an accurate replica of an incoming signal. For example, in a computer, a phase-locked loop is used by a microprocessor to generate an on-chip clock signal from an off-chip clock signal.

Thus, the teaching of Ho, on which the Office action relies, states that a phase-locked loop can receive an off-chip clock signal and generate an on-chip clock signal. In other words, Ho teaches, like the IBM reference cited before, that a phase-locked loop circuit can be connected to an off-chip clock signal. Ho neither teaches nor suggests that the buffered reference clock output (BUFREFCLK) of the first phase-locked loop circuit is electrically coupled to the on-chip reference clock input (REFCLK) of the second phase-locked loop circuit (PLL7SLIBI). In fact, applicants do not even see where within Ho a second phase-locked loop is taught, let alone the interconnection of two phase-locked loops as recited in independent claim 1.

For at least these reasons, applicants submit that the IBM reference, alone or in combination with Ho, neither teaches nor suggests all the claim elements and limitations as recited in claim 1. Additionally, as the Office action has applied the same rejection rational in rejecting independent claims 9, 15, 18 and 20, applicant applies these same arguments to overcome these rejections. Therefore, applicants request the rejections of claims 1, 9, 15, 18 and 20 be withdrawn, and claims 1, 9, 15, 18, and 20 be allowed as the prior art of record neither teaches nor suggests all the elements/limitations of these claims.

Additionally, dependent claims 2-8, 10-14, 16-17, and 19, are believed to be allowable for at least the reasons for allowance of their respective independent claims.

For at least these reasons, applicants request the rejections of claims 1-20 be withdrawn, and claims 1-20 be allowed.

CONCLUSION

In view of the above remarks, the application is considered in good and proper form for allowance, and the Examiner is respectfully requested to pass this application to issue. If, in the opinion of the Examiner, a telephone conference would expedite the prosecution of the subject application, the Examiner is invited to call the undersigned attorney.

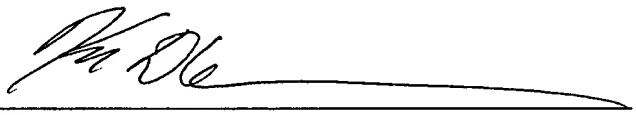
In re David Glen Roe
Application No. 09/814,244

The Commissioner is hereby generally authorized under 37 C.F.R. § 1.136(a)(3) to treat this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 requiring an extension of time as incorporating a request therefore, and the Commissioner is hereby specifically authorized to charge Deposit Account No. 501430 for any fee that may be due in connection with such a request for an extension of time.

The Commissioner is hereby authorized to charge payment of any fee due any under 37 C.F.R. §§ 1.16 and § 1.17 associated with this communication or any future communication in this or any related application filed pursuant to 37 C.F.R. § 1.53 or credit any overpayment to Deposit Account No. 501430.

Respectfully submitted,
The Law Office of Kirk D. Williams

Date: October 2, 2002

By 

Kirk D. Williams, Reg. No. 42,229
One of the Attorneys for Applicants
CUSTOMER NUMBER 26327
The Law Office of Kirk D. Williams
1234 S. OGDEN ST., Denver, CO 80210
303-282-0151 (telephone), 303-778-0748 (facsimile)